



Driver Optimization Method Based on Genetic Algorithm for IGBT

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Introduction

Genetic Algorithm Gate Driver (GAGD): A technique optimizing gate driving using genetic algorithms.

- * Gate characteristic testing platform with high bandwidth, voltage swing, and output speed.
- # Genetic algorithms generate gate voltage waveforms,

Genetic algorithms are employed to address the complexity and high degree of freedom in waveform generation.



drive IGBTs, and optimize output voltage waveform.

- Iterative optimization considering turn-on losses and stress.
- * Experimental comparisons with traditional techniques demonstrate favorable transient characteristics of the optimized drive mode.

Principle

- * GA program execution on PC for iterative waveform optimization.
- * Optimized waveform transmission to FPGA.
- Waveform processing through DA module.
 Stimulating driving circuit.
 Collecting and analyzing output signal using an oscilloscope.

Fig. 3. Waveform Sketches Used For IGBT Gate Driving Wave Form Optimization

Algorithm

- Iterative optimization process: Genetic algorithm mimics evolution.
 Encoding and generating initial population: Random voltage values.
 Individuals represent waveforms: Genes indicate voltage at time nodes.
 Waveform drives IGBT: Transient indicators for fitness evaluation.
 Higher fitness leads to selection: Crossover and mutation in next generation.
 Fitness evaluation for convergence: Factors like initial population and gene count.
 Adjustments based on application: Practical considerations.
- Cyclic repetition for comprehensive and reliable data collection.



Fig. 1. Hardware Platform Structure







$V_{G} \downarrow_{G} \downarrow_{G$

Fig. 4. Single Point Crossing Algorithm(Left), Mutation Algorithm(Right)

Fig. 2. Driver Board

The IGBT is FS35R12W1T4, paired with the ADA4870 which has high voltage swing rate and high output current performance. Its frequency is 125MHz.

In this paper, single-point crossover is used. The mutation probability randomly selects mutation positions and modifies the original voltage values to random voltages.





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Experimental environment

The experimental process selected the IGBT turn-on process, with a bus voltage of 400V, a load current of 12.5A, and a load inductance of 500uH.





Fig. 6. Driver Board(Left), Infineon evaluation board (Right)

Experimental Result

The black 'x' marks indicate the turn-on losses and current overshoot of the Infineon evaluation board in the results. The dot marks represent the turn-on wave-form data observed during the iteration process.



The black 'x' marks indicate the conduction losses and current overshoot of the resulting product A.

150

 $\dot{l}_{\rm C}({\rm A})$

20

15

10

5

-5



Fig. 8. Results Compared With Infineon's Evaluation Board





fineon Evaluation Board

	Turn-on Loss(mJ)	Current Spike(%)
GAGD	0.662	68.92
1ED3122Mx12H	0.78	67.56
Performance	0.118	1.32%

on product A

	Turn-on Loss(mJ)	Current Spike(%)
GAGD	1.36	28.5
Product A	2.41	18.7
Performance	1.05	9.8

Conclusion

Experimental results show improved transient performance of the optimized drive waveform compared to traditional gate drivers. However, it has limitations and further analysis and research are required before applying the optimization results in engineering.

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